XPedite2770

AMD (formerly Xilinx) Versal® Prime VM1402 ACAP-Based 3U VPX Module with 16 GB of LPDDR4, PCIe Gen3, and SecureCOTS™

- AMD (formerly Xilinx) Versal® Prime VM1402 ACAP

- 3U VPX (VITA 46) module

- Compatible with multiple VITA 65 OpenVPX™ slot profiles and SOSA-aligned options

- 16 GB of LPDDR4 ECC SDRAM in two channels

- 4 Gbit of QSPI FPGA configuration flash

- 32 GB of SLC NAND flash

- XMC site with one x8 PCI Express Gen2-capable interface (capable of PCIe Gen3 dependent on user application) and rear I/O support

- Two 10/100/1000BASE-T Ethernet ports

- Two GTY High-Speed Serial (HSS) lanes capable of 10GBASE-R Ethernet (contact X-ES for IP requirements)

- One x4 PCI Express Gen3-capable interface to P1.A

- One x4 PCI Express Gen2-capable interface to P1.B (capable of PCIe Gen3 dependent on user application)

- One x1 PCI Express Gen2-capable interface (capable of PCIe Gen3 dependent on user application)

- One RS-232/422/485 serial port

- One UART/RS-232 maintenance port

- 14 LVDS GPIO

- 16 single-ended (SE) GPIO

- Linux Yocto support

- FPGA Development Kit (FDK)

XPedite2770

The XPedite2770 is a high-performance, reconfigurable, conduction-cooled, 3U VPX processing module based on the AMD (formerly Xilinx) Versal® Prime Adaptive Compute Acceleration Platform (ACAP). With multiple high-speed fabric interfaces and 16 GB of LPDDR4 ECC SDRAM in two channels, the XPedite2770 is ideal for customizable, high-bandwidth, signal-processing applications. It integrates SecureCOTS™ technology with a Versal® Prime VM1402 ACAP for hosting custom functions to protect data from being modified or observed and provides an ideal solution when stringent security capabilities are required.

The XPedite2770 is a heterogeneous compute platform that delivers exceptional performance utilizing two ARM® Cortex®-A72 processor cores, two ARM® Cortex®-R5F real-time processor cores, a Network-on-Chip (NoC) interconnect, and a large FPGA fabric. These devices provide specialized processing elements designed to meet the demands of high-bandwidth applications such as packet processing, signal processing, sensor I/O, DSP-intensive applications, next-generation wired and 5G wireless infrastructure, cloud computing, and aerospace and defense applications.

Providing incredible speed with two x4 PCI Express interfaces and two 10/100/1000BASE-T Ethernet ports, the XPedite2770 accommodates up to 32 GB of onboard SLC NAND flash in addition to numerous I/O ports, including LVDS, single-ended GPIO, and RS-232/422/485 serial through the backplane connectors. The XPedite2770 provides additional expansion capabilities by including an integrated XMC site. This XMC site includes a x8 PCI Express connection to the Versal® Prime ACAP and X12d I/O mapped directly to the VPX backplane connectors. Additional configurations can route x16s and x8d from the XMC site to the VPX backplane connectors.

The XPedite2770 provides a high-performance, feature-rich solution capable of interfacing to and processing streaming data from a wide variety of sensors. The X-ES FPGA Development Kit (FDK) is provided to support the requirements of high-performance, real-time, embedded, streaming-data applications and simplify FPGA development. X-ES' FDK includes IP blocks, HDL, test benches, Linux Yocto support, and complete example designs for the XPedite2770.

X-ES
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"Fast, Flexible, Customer-Focused Embedded Solutions"

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FPGA

- AMD (formerly Xilinx) Versal® Prime VM1402 ACAP for high-performance logic and DSP applications
- Dual-core ARM® Cortex®-A72, 48 KB/32 KB L1 cache with parity and ECC; 1 MB L2 cache with ECC
- Dual-core ARM® Cortex®-R5F, 32 KB/32 KB L1 cache, and 256 KB TCM with ECC

Memory

- 16 GB of LPDDR4 ECC SDRAM in two channels
- 32 GB of SLC EMMC NAND flash
- 4 Gbit of QSPI FPGA configuration flash

XMC Site

- One x8 PCI Express Gen2-capable interface (capable of PCIe Gen3 dependent on user application)

VPX (VITA 46) P0 I/O

- Two IPMB connections to an IPMI controller

VPX (VITA 46) P1 I/O

- One x4 PCI Express Gen3-capable interface to P1.A
- One x4 PCI Express Gen2-capable interface to P1.B (capable of PCIe Gen3 dependent on user application)
- Two GTY High-Speed Serial (HSS) lanes capable of 10GBASE-R Ethernet (contact X-ES for IP requirements)
- XMC P16 I/O, mapping P1w9-X12d per VITA 46.9

VPX (VITA 46) P2 I/O

- Two 10/100/1000BASE-T Ethernet ports
- Six LVDS GPIO
- One x1 PCI Express Gen2-capable interface (capable of PCIe Gen3 dependent on user application) (contact X-ES for SATA support options)
- One RS-232/422/485 serial port
- Build option for eight LVDS and 16 SE GPIO from the FPGA, or XMC P16 I/O mapping P2w9-X16s+X8d

Development Support

- U-Boot firmware
- Linux Yocto support
- X-ES FPGA Development Kit (FDK)

Physical Characteristics

- 3U VPX-REDI conduction- or air-cooled form factor
- Dimensions: 100 mm x 160 mm
- 0.8 in. pitch without solder-side cover
- 0.85 in. and 1.0 in. pitch with solder-side cover and Two-Level Maintenance (2LM) support
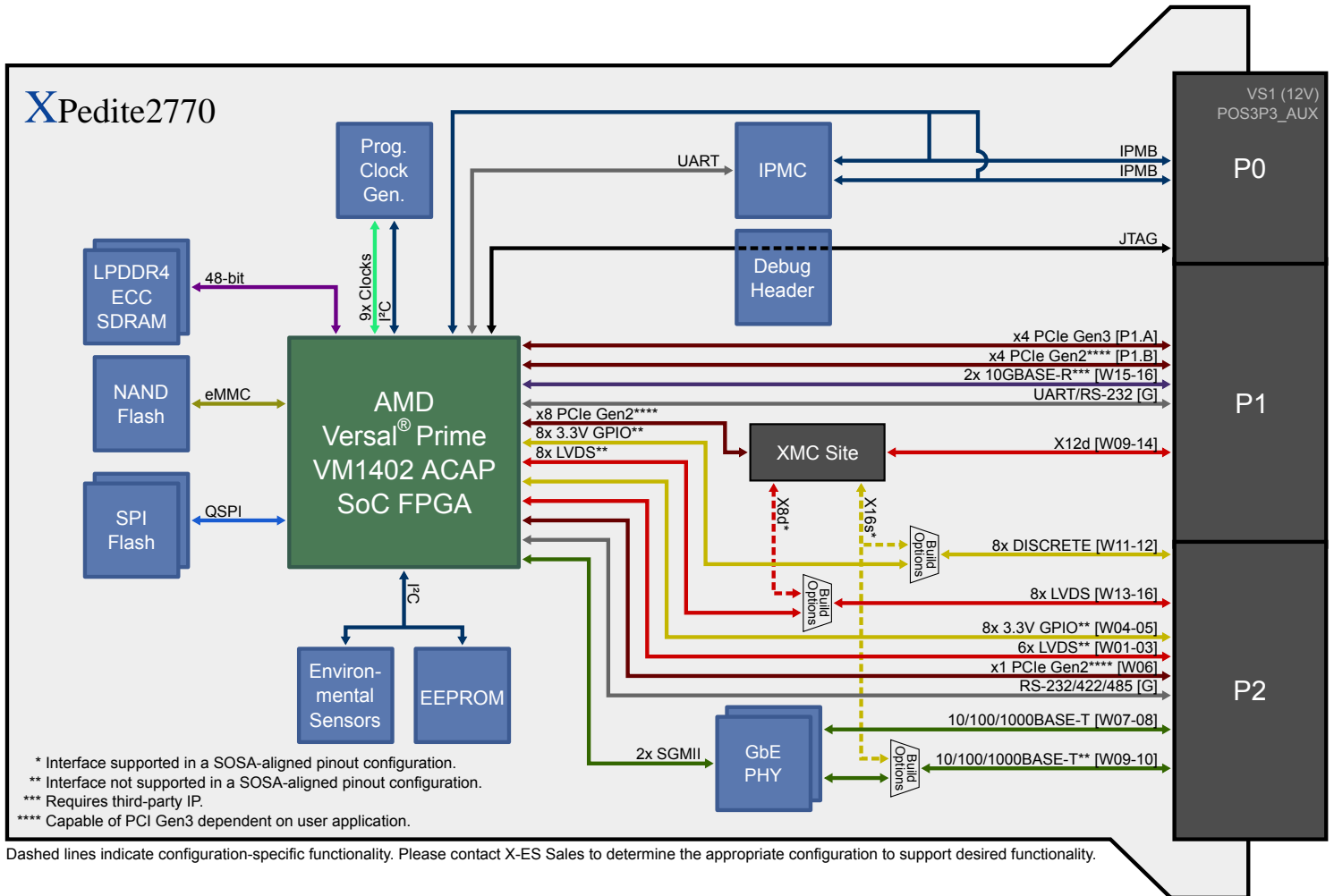
Environmental Requirements

Contact factory for appropriate board configuration based on environmental requirements.

- Supported ruggedization levels (see chart below): 5
- Conformal coating available as an ordering option

Power Requirements

- Power will vary based on configuration and usage. Please consult factory.

Ruggedization Level	Level 5
Cooling Method	Conduction-Cooled
Operating Temperature	-40 to +85°C (board rail surface)
Storage Temperature	-55 to +105°C (maximum)
Vibration	0.1 g²/Hz (maximum), 5 to 2000 Hz
Shock	40 g, 11 ms sawtooth
Humidity	Up to 95% non-condensing

* Interface supported in a SOSA-aligned pinout configuration.
** Interface not supported in a SOSA-aligned pinout configuration.
*** Requires third-party IP.
**** Capable of PCI Gen3 dependent on user application.

Dashed lines indicate configuration-specific functionality. Please contact X-ES Sales to determine the appropriate configuration to support desired functionality.