



## IF/Baseband Signal Sampling

## Board Features

- Dual 14-bit 500Mps ADCs
- External Clock Input

## Summary

The **XRM-ADC-D9/500** is an XRM2 I/O Module, providing two Analog to Digital converters with 14-bit resolution at sampling rates up to 500Mps.

Aimed at IF/Baseband Signal Sampling, the sampling clock can be sourced from either an external clock source or from a clock generated within the attached FPGA board. An Auxiliary I/O port is provided for use as a trigger input and general purpose signaling. An additional two ports are available for use as high-speed interconnect between boards for synchronisation.

## Deliverables

XRM2-ADC-D9/500 Board  
 One Year Warranty  
 One Year Technical Support

## Board Format

Alpha Data XRM2 I/O Module

## Input/Output Interfaces

### 2x Dual Analog to Digital Converters

Resolution: 14-bit  
 Max Sample Freq: 500Mps  
 Bandwidth: 4.5MHz to 700MHz  
 Impedance: 50Ω  
 Connector: SSMC

##Note:## exceeding the maximum signal limit may result in permanent degradation of converter performance.

### 1x External Clock Input

Impedance: 50Ω  
 Levels: +3V3 LVTTTL  
 Connector: SSMC

##Note:## Exceeding the maximum voltage limit may result in permanent degradation of converter

### 2x Auxiliary I/O

Impedance: 4k7Ω (DC Coupled)  
 Levels: 2V5 Logic (DC coupled)  
 Connector: SSMC

User configurable as inputs or outputs



**Support**

Example UCF, HDL files and Application software are provided with the board.

**Environmental Specification****Temperature Ranges**

Cooling Option	Operating Temperatures		Storage Temperatures	
	Min	Max	Min	Max
AC0	0°C	55°C	-40°C	85°C

Operating Humidity : Up to 95% (non-condensing)

**EMC Standards**

FCC 47CFR Part 2

EN55022:2010 Equipment ClassB

**Ordering Information****Order Code: XRM2-ADC-D9/500**

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